Serie 07 - Solution

Preamble

1.1 Work function

The **work function** W of a material is defined as the energy required to extract an electron from the Fermi level to the vacuum level. Essentially, if enough energy is supplied to an electron, it can be extracted from the material. A direct manifestation of this phenomenon can be seen in the photoelectric effect. When light is shone onto a metal, electrons are emitted if the photons have sufficient energy.

Conventionally, the vacuum level energy E_0 is defined as zero. Therefore, any particle that is gravitationally or electrically bound has negative potential energy, meaning it requires a positive energy to free it. Consequently, the work function is always positive.

$$W = \phi \cdot q = E_0 - E_f \tag{1}$$

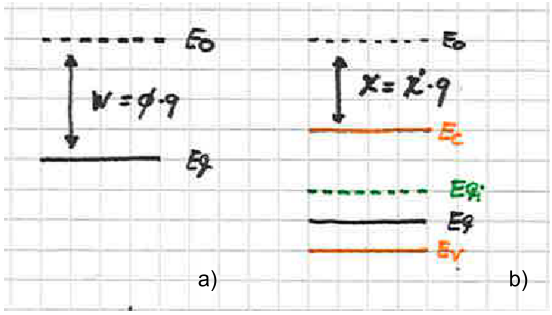

Figure 1: a) Working function. b) Electron affinity.

1.2 Electron affinity

As can be easily understood, the work function can be annoying to use in the case of a semiconductor. In a doped semiconductor, the Fermi level will change depending on the doping level, and hence the work function will also change. Therefore, in this case, we prefer to use the electron affinity instead.

The **electron affinity** χ is defined as the energy required to extract an electron from the conduction band level to the vacuum. Like the work function, the electron affinity is positive due to the convention of defining the vacuum level energy as zero.

$$\chi = \chi' \cdot q = E_0 - E_c \tag{2}$$

An illustration of the electron affinity can be found at Fig. 2.

1.3 Connecting Materials with Different Work Functions

In the same structure, the vacuum level and the Fermi level should always be continuous. Therefore, when we put two materials with different work functions in contact, we will see the creation of an electric field and the movement of charge. This will locally change the work function and "bend" the energy level to match the preceding conditions. The amplitude of this bending is necessarily equal to the difference in the work functions of the two materials. In the case of MOS structures, this will create the depletion region in the base and the accumulation of charges on the gate.

The most important parameter is the difference between the Fermi level and the other energy levels. Therefore, graphical representations can have multiple references. In this course, we prefer to keep the vacuum level constant. However, in other courses, especially ones which include band diagram drawing, they prefer to keep the Fermi level constant at 0 bias.

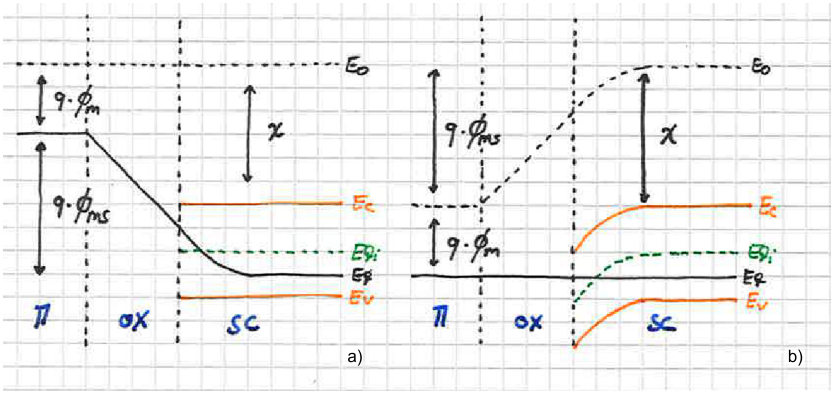

Figure 2: a) Constant E_0 convention used in the MOS structure in this course. b) Constant E_f convention used in the MOS structure.

1.4 Interfacial charges

During the course, you learned about the charge distribution in an ideal MOS structure. However, in reality, charges can get trapped in the oxide layer or at the junction between the base and the oxide. There are many factors that can lead to the appearance of these charges, such as wafer or oxide contamination during the fabrication process. These parasitic charges are known as interfacial

charges (Q_{ss}), and they can significantly impact the characteristics of the MOS structure. Even if some of the charges are trapped in the oxide, we model them by adding them at the junction between the oxide and the channel.

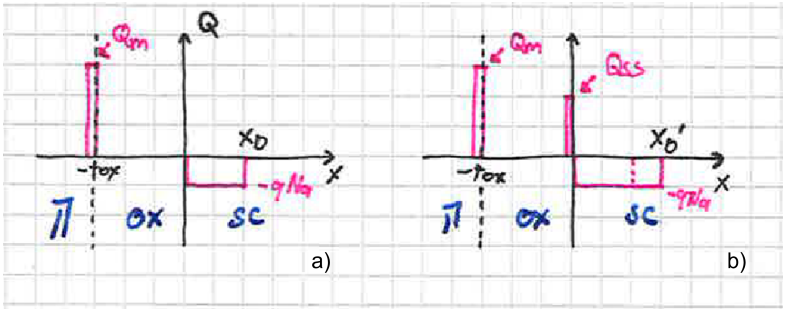

Figure 3: a) Ideal MOS structure without interfacial charges. b) Non-Ideal MOS structure with interfacial charges.

In Fig. 3, Q_{ss} and Q_m are shown as rectangles, but in reality, the interfacial charges Q_{ss} and the charge accumulated on the gate Q_m are closer to a Dirac function. These small rectangles are a graphical representation of these charges.

1.5 Sign convention

Here we want to quickly talk about the difference between "difference" and "drop". Let's take an example.

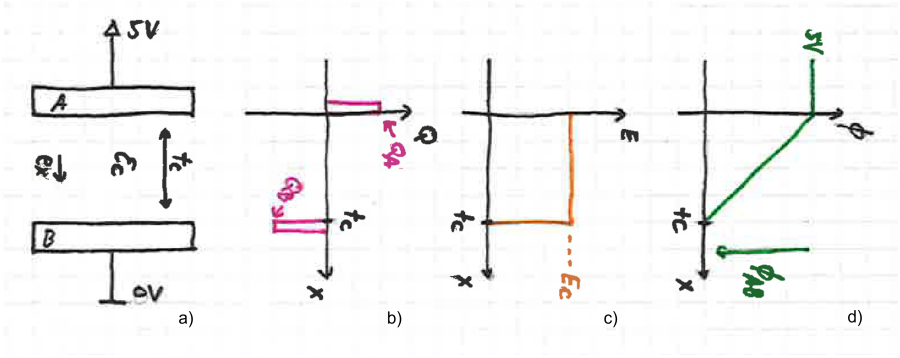

Figure 4: a) Capacitor topology. b) Charge distribution. c) Electric field distribution. d) Electric potential distribution.

Take a capacitor with plate A connected to a voltage of $5\,[V]$, and its plate B connected to ground. The two plates are separated by a distance t_c by an

insulator with a dielectric constant ϵ_c. As electrical students, you will all agree that the voltage difference between plates A and B will be $V_{AB} = 5\,[V]$. Now, we want to find this by integrating Maxwell's equations. In the capacitor, the electric field will be:

$$\vec{E_c} = \frac{Q_A}{\epsilon_c}\vec{e_x} \tag{3}$$

We now want to find the electric potential, and its physical definition is:

$$\phi = -\int \vec{E}\vec{dl} \tag{4}$$

If we integrate this over the capacitor:

$$\phi_{AB} = -\int_A^B E_c dx = -\int_0^{t_c} E_c dx = -\frac{Q_A}{\epsilon_c} \cdot x\Big|_{x=t_c}^{0} = -\frac{Q_A}{\epsilon_c} t_c \tag{5}$$

Since Q_A is positive, ϕ_{AB} is negative. This is because this is the calculation for the potential difference, which is, by definition, the inverse of the potential drop.

Because of this, knowing which sign to use can be a nightmare. In this exercise series, we will use ϕ (the only exception is the work function because of its definition) when we talk about differences, and V when we use drop. At the exam, you don't have to use this definition; the course doesn't use it either. We just use this to try to make the sign easier to find.

Here is a small table of correspondences between the course and this solution:

exercises	$\Rightarrow$	course
-ϕ_{ox}	$\Rightarrow$	V_{ox}
-ϕ_{sc}	$\Rightarrow$	V_b
-ϕ_b	$\Rightarrow$	ϕ_b

Given constants

$kT/q = 25.9\,[mV] \quad @ \quad T = 300\,[K]$
$n_i(Si) = 1.5 \cdot 10^{10}\,[cm^{-3}] \quad @ \quad T = 300\,[K]$
$q = 1.60 \cdot 10^{-19}\,[C]$
$\epsilon_0 = 8.85 \cdot 10^{-14}\,[F/cm]$
$\epsilon_{Si} = 11.7 \cdot \epsilon_0$
$\epsilon_{SiO} = 3.9 \cdot \epsilon_0$

Exercise 01

Calculate the work function difference between the metal and the semiconductor ϕ_{ms} in a MOS structure. The MOS structure is composed of an aluminum gate with a work function $\phi_m = 3.2\,[V]$ and a silicon channel with an electron affinity $\chi' = 3.25\,[V]$. We assume that the silicon has a band gap $E_g = 1.11\,[eV]$ and a doping concentration of $N_a = 10^{14}\,\left[cm^{-3}\right]$ and $n_i = 1.5 \cdot 10^{10}$.

Solution

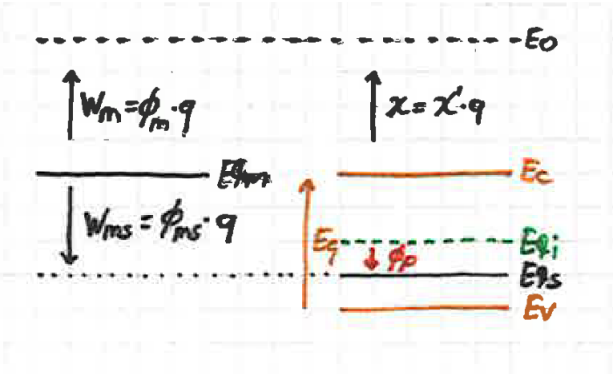

Figure 5: Drawing of the energy level in both structure.

We begin by calculating the work function of the semiconductor, denoted as W_s. To obtain this value, we first need to determine the energy difference between the conduction band and the Fermi level. We already have the electron affinity, denoted as χ', that is the difference between the conduction band and the vacuum level. In a previous series, we have demonstrated that the intrinsic Fermi level is located at the middle of the band gap.

$$E_{fi} - E_c \approx \frac{E_g}{2} \tag{6}$$

In a previous course, we have already seen the formula that gives the difference between the Fermi level and the intrinsic Fermi level, denoted as ϕ_p, depending on the carrier concentration. In our case, we have $p = N_a$.

$$\phi_p = -\frac{kT}{q} \ln\left(\frac{p}{n_i}\right) \approx -228\,[mV] \tag{7}$$

Hence:

$$W_s = \phi_s \cdot q = \chi' \cdot q + \frac{E_g}{2} - \phi_p \cdot q \tag{8}$$

And finally:

$$W_{ms} = E_s - E_m = E_s - E_0 + E_0 - E_m = W_m - W_s \tag{9}$$

$$\phi_{ms} = \frac{W_m - W_s}{q} = \phi_m - \left(\chi' + \frac{E_g}{2q} - \phi_p\right) \approx -833\,[mV] \tag{10}$$

In this type of exercise, be really careful about the signs.

Exercise 02

Calculate the maximum width of the Space Charge Region (SCR) in a MOS structure. The doping concentration of the semiconductor is $N_a = 10^{16}\left[cm^{-3}\right]$, the temperature is $T = 300\,[K]$, and we assume $n_i = 1.5 \cdot 10^{10}\left[cm^{-3}\right]$.

Solution

We will provide an explanation for a MOS structure based on a p-type semiconductor, as described in this exercise. However, the same logic can be easily applied to a MOS structure based on an n-type semiconductor.

As we discussed in the course, when the gate is biased, the depletion width increases until the threshold voltage is reached. At this point, further depletion of holes stops and a layer of electrons is created close to the oxide. In other words, when the threshold voltage is reached, the width of the space charge region (SCR) stops increasing.

The threshold voltage is reached when the potential built up in the space charge region ϕ_{sc} or V_B is equal to $2\phi_p$. The potential built up in the space charge region is given by the following formula:

$$\phi_{sc} = -\frac{qN_aX_D^2}{2\epsilon_{sc}} \tag{11}$$

As in the previous exercises, ϕ_p is given by the following equation where $p = N_a$.

$$\phi_p = -\frac{kT}{q}\ln\left(\frac{p}{n_i}\right) \approx -347\,[mV] \tag{12}$$

As explained earlier, $\phi_{sc} = 2\phi_p$, and we just have to extract X_D.

$$X_{Dth} = \sqrt{-\frac{2 \cdot 2\phi_p \cdot \epsilon_{sc}}{qN_a}} \approx 300\,[nm] \tag{13}$$

Exercise 03

Calculate the flat-band voltage V_{FB} of a MOS structure based on p-type silicon doped with $N_a = 10^{16}\left[cm^{-3}\right]$. The structure has a silicon oxide layer with a thickness of $t_{ox} = 50\,[nm]$, and a gate made of n+ doped polysilicon. We assume a work function difference between the metal and the semiconductor of $\phi_{ms} = -1.1\,[V]$ and an interfacial charge density of $Q_{ss} = 10^{11}\left[cm^{-2}\right]$.

Solution

In the course, the flat-band voltage has been defined as the gate-source bias voltage V_{gs} needed to just wipe out the SCR. In other words, the flat-band voltage occurs when no built-in potential appears in the semiconductor, i.e., no band bending.

In this exercise, we are dealing with a MOS structure based on a p-type semiconductor and with positive interfacial charges. The addition of these charges will change the electric field and, therefore, the distribution of the potential. In all cases, the built-in potential of the MOS should always be ϕ_{ms}. In Fig.6 d) (green), we can see a case where we have applied a gate-source bias voltage of $V_{gs} = \phi_{ms}$ in a non-ideal MOS structure that contains interfacial charges. We clearly see a built-in potential in the semiconductor and a bending of the potential in the region, implying a SCR.

To solve this exercise, we will draw the charge redistribution in the MOS structure in the flat-band and derive the electric field and the built-in potential.

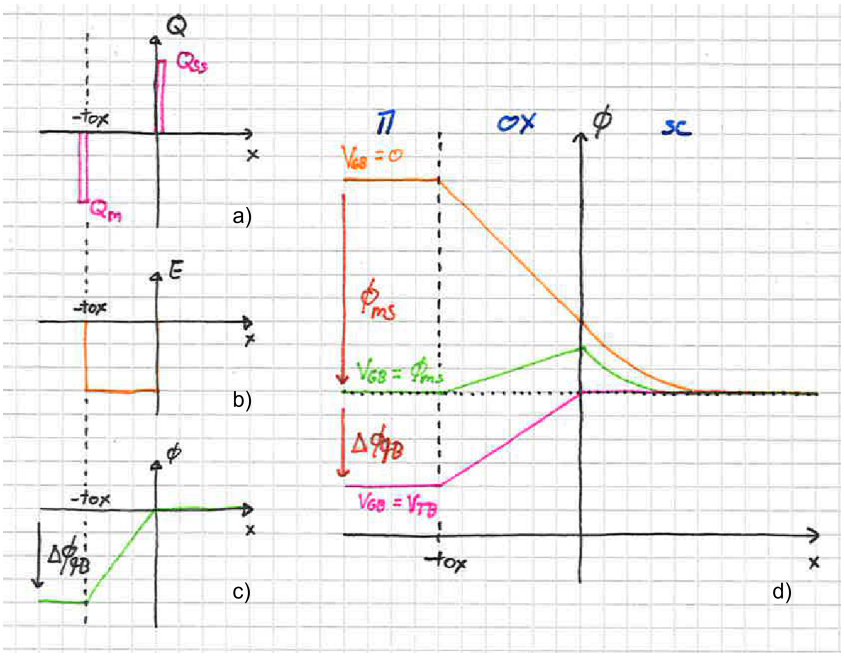

Figure 6: a) Charges in MOS structure at $V_{bg} = V_{FB}$. b) Electric field in MOS structure at $V_{bg} = V_{FB}$. c) Potential in MOS structure at $V_{bg} = V_{FB}$. d) Potential in MOS structure for different bias.

$$Q(x) = Q_m \cdot \delta(x + tox) + Q_{ss} \cdot \delta(x) \tag{14}$$

Where $\delta()$ is of course the Dirac function.

$$E(x) = \begin{cases} \frac{Q_m}{\epsilon_{ox}} & , \quad \text{if } x \in [-t_{ox}; 0] \\ 0 & , \quad \text{else} \end{cases} \tag{15}$$

$$\phi(x) = \begin{cases} \Delta\phi_{FB} & , \quad \text{if } x \in]\leftarrow; -t_{ox}] \\ -\frac{Q_m}{\epsilon_{ox}} \cdot x & , \quad \text{if } x \in [-t_{ox}; 0] \\ 0 & , \quad \text{else} \end{cases} \tag{16}$$

The overall MOS structure must be neutral. In this case, $Q_m = -Q_{ss}$; therefore:

$$\Delta\phi_{FB} = -Q_{ss}\frac{t_{ox}}{\epsilon_{ox}} = -\frac{Q_{ss}}{C_{ox}} \tag{17}$$

Finally:

$$C_{ox} = \frac{\epsilon_0 \epsilon_{oxr}}{t_{ox}} \approx 69\left[nF/cm^2\right] \tag{18}$$

Be careful! During the derivation of $\Delta\phi_{FB}$, Q_{ss} was the interfacial charge quantity, but the charge used in the calculations should be qQ_{ss}, where q is the elementary charge.

$$qQ_{ss} \approx 16\left[nC/cm^2\right] \tag{19}$$

$$V_{FB} = \phi_{ms} + \Delta\phi_{FB} = \phi_{ms} - \frac{qQ_{ss}}{C_{ox}} \approx -1.33\,[V] \tag{20}$$

Solution bis

Another method to obtain the same result is to recognize that at flat band, the interfacial charges are neutralized by the charge stored on the gate. In this case, we simply need to determine the additional voltage required to store the appropriate amount of charge on the gate. Since the MOS structure acts as a capacitor in this scenario, we have:

$$Q = C \cdot U \tag{21}$$

In this case $Q = Q_{ss}$, $C = C_{ox}$ and $U = -\Delta\phi_{FB}$.